

<b>Name of the Faculty: Ms. Jaya</b>
<b>Discipline: Computer science &amp; Engg.</b>
<b>Semester:5th</b>
<b>Subject: Computer Organization &amp; Architecture(CSE 307N)</b>
<b>Work Load (Lecture/Practical) per week (in hours): Lectures- 3 Hours , Practicals- 3 Hours</b>

Week	Theory	
	Lecture day	Topic (including assignment/test)
1 <sup>st</sup>	1 <sup>st</sup>	<b>Data representation and Computer arithmetic:</b> Introduction to Computer Systems
	2 <sup>nd</sup>	<b>Data representation and Computer arithmetic:</b> Organization and architecture
	3 <sup>rd</sup>	<b>Data representation and Computer arithmetic:</b> evolution and computer generations
2 <sup>nd</sup>	4 <sup>th</sup>	<b>Data representation and Computer arithmetic:</b> Fixed point representation of numbers
	5 <sup>th</sup>	<b>Data representation and Computer arithmetic:</b> digital arithmetic algorithms for Addition, Subtraction(Assignment-1)
	6 <sup>th</sup>	<b>Data representation and Computer arithmetic:</b> Multiplication using Booth's algorithm and Division using restoring and non restoring algorithms.
3 <sup>rd</sup>	7 <sup>th</sup>	<b>Data representation and Computer arithmetic:</b> Floating point representation with IEEE standards and its arithmetic operations.
	8 <sup>th</sup>	<b>Data representation and Computer arithmetic:</b> Floating point representation with IEEE standards and its arithmetic operations.
	9 <sup>th</sup>	Revision unit I
4 <sup>th</sup>	10 <sup>th</sup>	<b>Unit Test I</b>
	11 <sup>th</sup>	<b>Basic Computer organization and Design:</b> Introduction
	12 <sup>th</sup>	<b>Basic Computer organization and Design:</b> Instruction codes
5 <sup>th</sup>	13 <sup>th</sup>	<b>Basic Computer organization and Design:</b> stored program organization
	14 <sup>th</sup>	<b>Basic Computer organization and Design:</b> computer registers and common bus system
	15 <sup>th</sup>	<b>Basic Computer organization and Design:</b> computer instructions, timing and control, (Assignment-2)
6 <sup>th</sup>	16 <sup>st</sup>	<b>Basic Computer organization and Design:</b> instruction cycle: Fetch and Decode, (Assignment-2)
	17 <sup>nd</sup>	<b>Basic Computer organization and Design:</b> Register reference instructions; Memory reference instructions.
	18 <sup>rd</sup>	<b>Basic Computer organization and Design:</b> Input, output and Interrupt: configuration, instructions,
7 <sup>th</sup>	19 <sup>th</sup>	<b>Basic Computer organization and Design:</b> Program interrupt, Interrupt cycle,
	20 <sup>th</sup>	<b>Basic Computer organization and Design:</b> Micro programmed Control organization,
	21 <sup>th</sup>	<b>Basic Computer organization and Design:</b> address sequencing, micro instruction format and microprogram sequencer.
8 <sup>th</sup>	22 <sup>th</sup>	<b>Unit Test II</b>
	23 <sup>th</sup>	<b>Central Processing Unit:</b> Introduction
	24 <sup>st</sup>	<b>Central Processing Unit:</b> General register organization, stack organization
9 <sup>th</sup>	25 <sup>rd</sup>	<b>Central Processing Unit:</b> instruction formats,
	26 <sup>th</sup>	<b>Central Processing Unit:</b> addressing modes

	27 <sup>th</sup>	<b>Central Processing Unit:</b> , Data transfer and manipulation,
10 <sup>th</sup>	28 <sup>th</sup>	<b>Central Processing Unit:</b> Program control
	29 <sup>th</sup>	<b>Central Processing Unit:</b> CISC and RISC: features and comparison. (Assignment -3)
	30 <sup>th</sup>	<b>Central Processing Unit:</b> Pipeline and vector Processing
	31 <sup>st</sup>	<b>Central Processing Unit:</b> Parallel Processing, Pipelining
11 <sup>th</sup>	32 <sup>nd</sup>	<b>Central Processing Unit:</b> Instruction Pipeline
	33 <sup>rd</sup>	<b>Central Processing Unit:</b> Basics of vector processing and Array Processors.
12 <sup>th</sup>	34 <sup>th</sup>	<b>Unit Test III</b>
	35 <sup>th</sup>	<b>Input-output organization:</b> Introduction
	36 <sup>th</sup>	<b>Input-output organization:</b> I/O interface. I/O Bus and interface modules
13 <sup>th</sup>	37 <sup>th</sup>	<b>Input-output organization:</b> I/O versus Memory Bus.
	38 <sup>th</sup>	<b>Input-output organization:</b> Asynchronous data transfer: Strobe control, Handshaking
	39 <sup>st</sup>	<b>Input-output organization:</b> Asynchronous serial transfer
14 <sup>th</sup>	40 <sup>rd</sup>	<b>Input-output organization:</b> Modes of Transfer: Programmed I/O, Interrupt driven I/O
	41 <sup>th</sup>	<b>Input-output organization:</b> ., Priority interrupt; Daisy chaining, Parallel Priority interrupt.
	42 <sup>th</sup>	<b>Input-output organization:</b> Direct memory Access, DMA controller and transfer
15 <sup>th</sup>	43 <sup>th</sup>	<b>Input-output organization:</b> Input output Processor , CPU-IOP communication, I/O channel.
	44 <sup>th</sup>	<b>Input-output organization:</b> Input output Processor , CPU-IOP communication, I/O channel.
	45 <sup>th</sup>	<b>Unit Test IV</b>