Name of the Faculty: Mr. Hitesh Taluja
Discipline: Computer Science & Engineering
Semester:3rd Sem
Subject: Digital Electronics(CSE-207N)
Work Load (Lecture/Practical) per week (in hours): Lectures- 3 , Practicals- 3 Hours

	Theory		Practical	
Week	**Lecture day**	**Topic (including assignment/test)**	**Practical day**	**Topic**
1st	**1st**	Minimization Techniques: Boolean postulates and laws	**1st**	Familiarization with Digital Trainer Kit and associated equipment.
	2nd	De-Morgan's Theorem, Principle of Duality		
	3rd	Boolean expression - Minimization of Boolean expressions		
2nd	**4th**	Minterm, Maxterm, Sum of Products (SOP)	**2nd**	Study of TTL gates AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR.
	5th	Product of Sums (POS)		
	6th	Karnaugh map Minimization - Don't care conditions		
3rd	**7th**	Quine - McCluskey method of minimization	**3rd**	Study of TTL gates AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR.
	8th	Logic Gates: AND, OR		
	9th	NOT, NAND, NOR		
4th	**10th**	Exclusive-OR and Exclusive-NOR	**4th**	Design and realize a given function using K-Maps and verify its performance
	11th	Implementations of Logic Functions using gates		
	12th	NAND-NOR implementations		
5th	**13th**	Multi level gate implementations- Multi output gate implementations	**5th**	To verify the operation of Multiplexer and De-multiplexer
	14th	TTL and CMOS Logic and their characteristics,Tristate gates.		
	15th	Revision		
6th	**16th**	Class Test	**6th**	To verify the operation of Comparator.
	17th	Design procedure - Half adder, Full Adder		
	18th	Parallel binary adder, parallel binary Subtractor		
7th	**19th**	Fast Adder, Carry Look Ahead adder, Serial Adder/Subtractor	**7th**	To verify the truth table of S-R, J-K, T, D Flip-flops
	20th	BCD adder, Binary Multiplier, Binary Divider		
	21st	Multiplexer/ De-multiplexer, decoder, encoder		
8th	**22nd**	parity checker, parity generators, code converters, Magnitude Comparator	**8th**	To verify the truth table of S-R, J-K, T, D Flip-flops
	23rd	Revision		
	24th	Class Test		
	25th	Latches, Flip-flops - SR, JK, D, T		To verify the operation of Bi-directional shift register

9th	26th	Master-Slave - Characteristic table and equation, Application table	9th	
	27th	Edge triggering, Level Triggering, Realization of one flip-flop using other flip-flops		
10th	28th	serial adder/subtractor, Asynchronous Ripple or serial counter,	10th	To design and verify the operation of 3-bit asynchronous counter
	29th	Synchronous counters, Synchronous Up/Down counters, Programmable counters		
	30th	Design of Synchronous counters: state diagram, State table, State minimization		
11th	31st	State assignment, Excitation table and maps-Circuit implementation	11th	To design and verify the operation of asynchronous Up/down counter using J-K FFs
	32nd	Modulo-n counter, 555 Timer, Registers		
	33rd	shift registers, Universal shift registers, Shift register counters		
12th	34th	Ring counter, Shift counters, Sequence generators.	12th	To design and verify the operation of asynchronous Decade counter
	35th	Classification of memories - ROM: ROM organization, PROM, EPROM, EEPROM, EAPROM		
	36th	Revision		
13th	37th	Class Test	13th	Study of TTL logic family characteristics
	38th	RAM: - RAM organization - Write operation, Read operation		
	39th	Memory cycle, Timing wave forms, Memory decoding, memory expansion		
14th	40th	Static RAM Cell, Bipolar RAM cell, MOSFET RAM cell structure	14th	Study of Encoder and Decoder
	41st	Dynamic RAM cell structure, Programmable Logic Devices - Programmable Logic Array (PLA)		
	42nd	Programmable Array Logic (PAL), Implementation of PLA		
15th	43rd	PAL using ROM. Introduction to Field Programmable Gate Arrays (FPGA)	15th	Study of BCD to 7 segment Decoder
	44th	Revision		
	45th	Class Test		