# Lesson Plan

**Name of the Faculty: Ms. Reena Antil**

**Discipline: Aeronautical Engineering**

**Semester: 5th**

**Subject: Microprocessor and Interfacing**

**Work Load (Lecture/Practical) per week (in hours): Lectures- , Practicals- 0**

| Week | Theory | | Practical | |
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| | Lecture day | Topic (including assignment/test) | Practical day | Topic |
| 1st | 1st | Evolution of microprocessors, | 1st | |
| | 2nd | technological trends in microprocessor development. | | |
| | 3rd | The Intel family tree. | | |
| | 4th | CISC Versus RISC. | | |
| 2nd | 5th | Applications of Microprocessors. | 2nd | |
| | 6th | 8086 CPU ARCHITECTURE : | | |
| | 7th | 8086 Block diagram; | | |
| | 8th | description of data registers, address registers; pointer and index registers, | | |
| 3rd | 9th | description of data registers, address registers; pointer and index registers, | 3rd | |
| | 10th | PSW, Queue, BIU and EU. | | |
| | 11th | 8086 Pin diagram descriptions. Generating 8086 CLK and reset signals using 8284. | | |
| | 12th | WAIT state generation. | | |
| 4th | 13th | Microprocessor BUS types and buffering techniques, | 4th | |
| | 14th | 8086 minimum mode and maximum mode CPU module. | | |
| | 15th | 8086 minimum mode and maximum mode CPU module. | | |
| | 16th | **Revision and Assignments** | | |
| 5th | 17th | **Test** | 5th | |
| | 18th | 8086 INSTRUCTION SET : Instruction formats, | | |
| | 19th | addressing modes, | | |
| | 20th | Data transfer instructions, | | |
| 6th | 21st | string instructions, | 6th | |
| | 22nd | logical instructions, | | |
| | 23rd | arithmetic instructions, | | |
| | 24th | transfer of control instructions; | | |
| 7th | 25th | process control instructions; | 7th | |

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| | **26th** | Assembler directives. | | |
| | **27th** | 8086 PROGRAMMING TECHNIQUES : Writing assembly Language programs for logical processing, arithmetic processing, timing delays; | | |
| | **28th** | loops, data conversions. | | |
| **8th** | **29th** | Writing procedures; | **8th** | |
| | **30th** | Data tables, modular programming. Macros. | | |
| | **31st** | **Revision and Assignment** | | |
| | **32nd** | **Test** | | |
| **9th** | **33rd** | MAIN MEMORY SYSTEM DESIGN : Memory devices, | **9th** | |
| | **34th** | 8086 CPU Read/Write timing diagrams in minimum mode and maximum mode. | | |
| | **35th** | 8086 CPU Read/Write timing diagrams in minimum mode and maximum mode. | | |
| | **36th** | Address decoding techniques. | | |
| **10th** | **37th** | Address decoding techniques. | **10th** | |
| | **38th** | Interfacing SRAMS; | | |
| | **39th** | ROMS/PROMS. Interfacing and refreshing DRAMS. | | |
| | **40th** | ROMS/PROMS. Interfacing and refreshing DRAMS. | | |
| **11th** | **41st** | DRAM Controller – TMS4500. | **11th** | |
| | **42nd** | DRAM Controller – TMS4500. | | |
| | **43rd** | **Revision and Assignments** | | |
| | **44th** | **Test** | | |
| **12th** | **45th** | BASIC I/O INTERFACE : Parallel and Serial I/O Port design and address decoding. | **12th** | |
| | **46th** | Memory mapped I/O Vs Isolated I/O Intel's 8255 and 8251- description and interfacing with 8086. | | |
| | **47th** | Memory mapped I/O Vs Isolated I/O Intel's 8255 and 8251- description and interfacing with 8086. | | |
| | **48th** | ADCs and DACs, - types, operation and interfacing with 8086. | | |
| **13th** | **49th** | ADCs and DACs, - types, operation and interfacing with 8086. | **13th** | |
| | **50th** | Interfacing Keyboards, alphanumeric displays, multiplexed displays, and high power devices with 8086. | | |
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|---|---|---|---|---|
| | | alphanumeric displays, multiplexed displays, and high power devices with 8086. | | |
| | **52nd** | Interfacing Keyboards, alphanumeric displays, multiplexed displays, and high power devices with 8086. | | |
| **14th** | **53rd** | INTERRRUPTS AND DMA : Interrupt driven I/O. | **14th** | |
| | **54th** | 8086 Interrupt mechanism; | | |
| | **55th** | interrupt types and interrupt vector table. | | |
| | **56th** | interrupt types and interrupt vector table. | | |
| **15th** | **57th** | Intel's 8259. DMA operation. | **15th** | |
| | **58th** | Intel's 8237. Microcomputer video displays. | | |
| | **59th** | **Revision and Assignments** | | |
| | **60th** | **Test** | | |